A Vertically Integrated High Resolution Active Pixel Image Sensor for Deep Submicron CMOS Processes

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Abstract

A novel high resolution active pixel sensor in TFA technology has been fabricated. TFA technology [1] employs an amorphous silicon (a-Si:H) based thin film detector on top of an ASIC. The two components can be optimized independently of each other, and fill factors of up to 100 % are feasible. The presented prototype has been developed for digital photography and includes two different pixel variants and CDS/DDS circuits for efficient Fixed Pattern Noise (FPN) correction on-chip.

Introduction

The rapidly growing market of digital photography primarily requires image sensors with high pixel counts. Furthermore, integrating most of the image processing on-chip is desirable with respect to data rate, storage capacity and power consumption. The commonly employed CCD sensors are limited to serial readout and are able to provide raw image data only. CMOS sensors allow on-chip image processing, however, they suffer from the lateral integration of photodetector and pixel circuitry that have to share the pixel area. Moreover, the ASIC process can only be optimized for either the optical detector or the electronics. TFA technology offers a remedy to solve this conflict. It allows 3D integration of detector and pixel electronics by deposition of an amorphous silicon photoconversion layer on top of a standard ASIC (Fig. 1).

Fig.1: Basic structure of a TFA sensor

Another substantial advantage of TFA, in particular for small pixels and thereby for high pixel counts, becomes evident, as ASIC processes are continuously scaled down. The required shallower depletion regions and higher substrate doping for deep submicron processes will lead to a great sensitivity loss in CMOS sensors [2]. In contrast, the thin film detector of a TFA sensor is fabricated independently of the ASIC and is therefore not affected by ASIC scaling. Along with the inherent 3D structure of a TFA sensor a higher integration density than with any other existing technology may be accomplished. A high resolution image sensor concept in TFA technology has the best potential for the development of powerful and cost effective megapixel sensors with on-chip image processing for both volume and high end applications.

HIRISE II (High Resolution Image Sensor)

HIRISE II is an active pixel test chip with three sensor arrays. The first array includes 1024 rows and 128 columns for the test of long readout lines, the second has 128 rows and 1024 columns for the test of long row selection lines. The third array consists of 128 × 128 pixels. A block diagram of HIRISE II is given in Fig. 2.
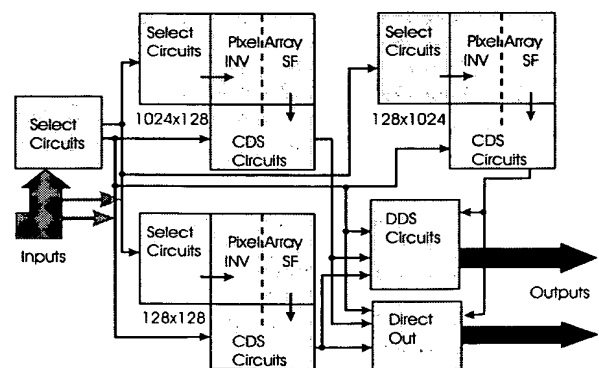

Fig. 2: Block diagram of the HIRISE II

HIRISE II is operated in slit shutter mode, implying that the exposure period is shifted from row to row, as opposed to a common integration period for all rows. The latter mode would require an additional integration start/stop transistor per pixel, leading to a higher area consumption.

Fig. 3 shows slit mode timing diagrams for two exposure periods. In order to avoid overexposure, the exposure time can be globally adapted to the illumination intensity by means of an additional reset (electronic shutter), as depicted in the lower diagram.
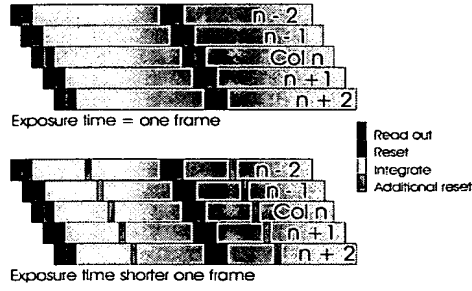

Exposure time = one frame

Read out
Reset
Integrate
Additional reset

Exposure time shorter one frame

Fig. 3: Exposure diagram for HIRISE II

A. The pixels

Each array includes two pixel variants. The first variant employs an inverter readout circuit and is implemented in the left half of each array. The second one is a source follower readout and can be found in the right half. Both pixel versions consist of three transistors, a reset transistor M1, a readout transistor M2 and a driver transistor M3. The integration capacitor is realized in the form of the combined parasitic capacitances of the amorphous photodiode and the ASIC circuitry. The schematics are given in Fig. 4 for inverter readout and Fig. 5 for source follower readout.
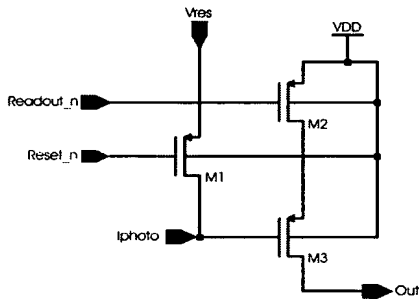
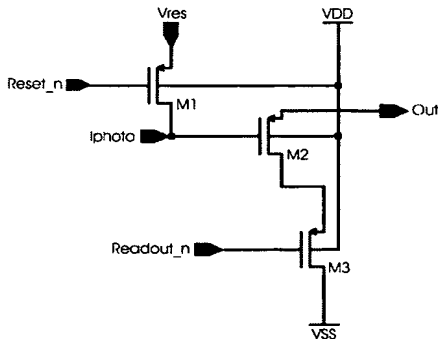

Fig. 4: Pixel schematic with inverter readout

Fig. 5: Pixel schematic with source follower readout

The two pixel options have been implemented for a comparative test of sensitivity, linearity and fixed pattern noise insensitivity.

The design is realized in a 0.8μm 2M2P CMOS process provided by AMS. For the sake of minimizing the pixel area the row selection line is completely implemented in the poly1 layer, and the pixels contain PMOS transistors only. The pixel variants share a common row selection line. The layouts are given in Fig. 6 and Fig. 7, respectively.
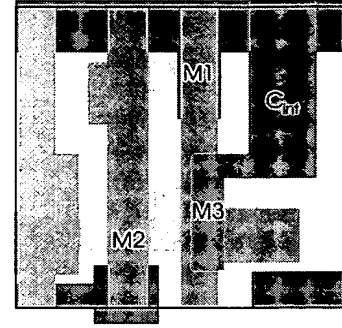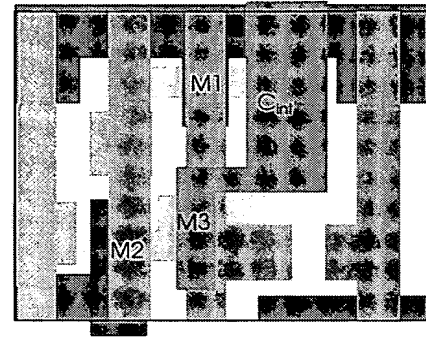

Fig. 6: Pixel layout with inverter readout

Fig. 7: Pixel layout with source follower readout

The area of the inverter readout pixel is 10 μm × 10 μm, while the source follower readout requires 10 μm × 12 μm.

B. The readout circuits

The readout circuits include CDS (Correlated Double Sampling) and DDS (Double Delta Sampling) to suppress fixed pattern noise [3]. CDS is performed for each column amplifier, whereupon DDS is implemented along with the pad driver once per array and per pixel variant. The principle of a CDS/DDS circuit is illustrated in Fig. 8.

In a first step the integration value V_{int} is read out from the pixel. At this time the switch M2 is closed. The left plate of the capacitor C1 holds V_{int}, while the second one is clamped to V_{refl}. After M2 has been opened, the integration capacitance inside the pixel is reset and the potential of the left plate will change to the pixel reset value V_{res}. The potential of the right plate is now given by

$$V_{col} = V_{refl} - V_{pix}, \qquad (1)$$

where V_{pix} denotes the effective integration voltage

$$V_{pix} = V_{int} - V_{res}, \qquad (2)$$

cleared of the reset voltage and pixel amplifier induced FPN in the form of threshold voltage variations.

For the elimination of column fixed pattern noise predominantly due to M3/M4, V_{col} is read out onto the left plate of C2, while the switch M5 is closed. As M5 is opened again and M2 is closed, the left plate of C2 is on V_{refl} potential. The output voltage is now

$$V_{out} = a (V_{refl}* - V_{col}*) \qquad (3)$$

where a is the amplifier gain, given by the capacitive division ratio of C2 and C3, and the asterisk denotes FPN affected voltages. The subtraction largely eliminates this FPN.
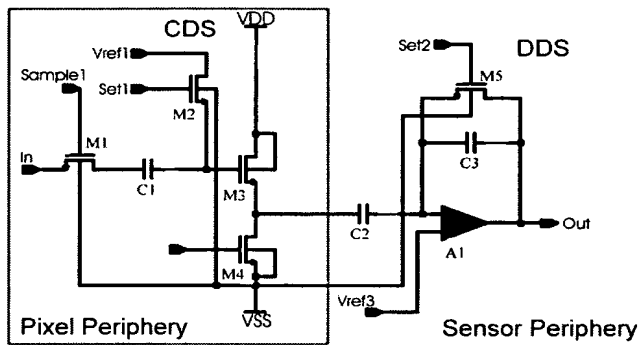

Fig. 8: Schematic of CDS and DDS circuits

C. The photodetectors

The photodetectors are realized using an a-Si:H thin film system. Two thin film variants have been implemented. The first variant is a nip structure which makes use of the metal2 layer of the ASIC process as the diode rear electrode. The second option is a metal-ip-TCO structure. This layer system requires an additional chromium layer as the diode rear contact. The structures are deposited on top of the ASIC in a low cost, low temperature PECVD process. No patterning of the thin film system is necessary.
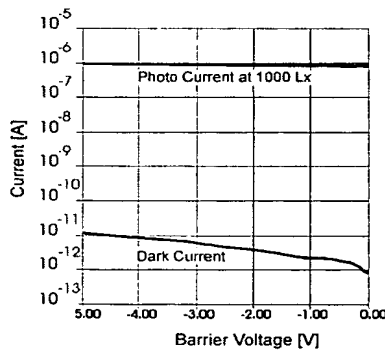

Fig. 9: Dark and photo current of metal-ip-TCO diode

Since the highly doped low resistive n-layer is missing, the metal-ip-TCO system provides better local contrast than the nip type. However, either diode achieves a dynamic range above 100 dB referred to 1000 lx illumination intensity. Fig. 9 shows the dark current and the photo-current at 1000 lx measured for a metal-ip-TCO diode.

D. Chip geography

Fig. 10 shows a photograph of the HIRISE II chip. The die size of the entire chip is 16.6 mm x 12.6 mm.

The structures 1.1/1.2 show the 1024 lines x 128 columns array and corresponding CDS circuits while 2.1/2.2 and 3.1/3.2 belong to the 128 lines x 1024 columns array and the 128 x 128 test array and corresponding CDS circuitry. Block 4 contains various test circuits.
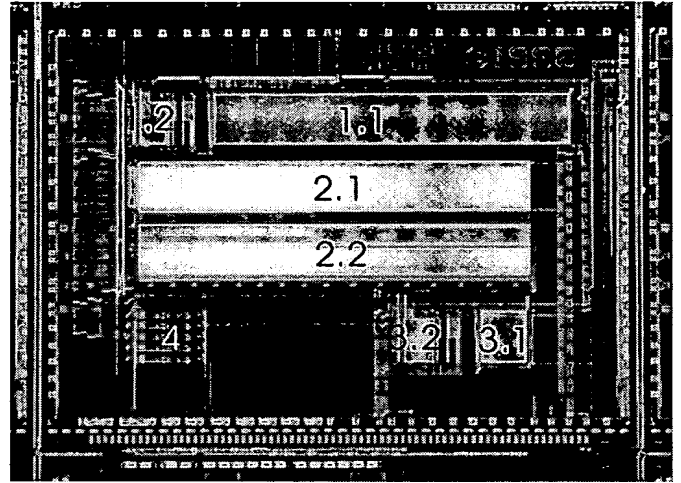

Fig. 10: Photograph of HIRISE II chip

E. Results

First measurements have been carried out with the HIRISE II at a frame rate of 130 Hz, reading out 128 × 495 pixels. The integration period was 7,6 ms.

The noise floor was found to be below 2 mV_{rms}, while the full scale voltage is 2.5 V. This yields a dynamic range of more than 60 dB. The output referred sensitivity is 8.6 V lx^{-1} sec^{-1} for the inverter readout circuit.

Fig. 11 shows an image of a black-and-white line pattern (USAF 1951 test chart) for the evaluation of the local contrast of HIRISE II. The pattern was adjusted in a way that one line corresponded with one pixel row of the sensor. The local contrast, given by the ratio of bright to dark pixel signals, is 30 dB. Taking into account adjustment inaccuracy, the actual value may be still higher.

Measurements revealed a logarithmic ramp in the readout values of one row. Due to the high resistivity of the row-wise polysilicon line the reset clock slope is much steeper for the first pixels of the row than for the subsequent pixels. While the clock feedthrough due to the gate-drain/source overlap capacitances is the same for all pixels, the channel charge distribution while switching off

changes with the switching speed, leading to different reset voltage offsets within the row. Fortunately, this effect can be corrected with the CDS circuits.
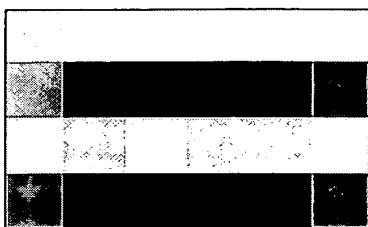

Fig. 11: Local contrast

Images taken with the HIRISE II are given in Fig. 12 and Fig. 13, with 128 × 495 and 495 × 128 pixels resolution, respectively.

Fig. 12: Image taken with HIRISE II

Conclusion

A high resolution image sensor in TFA technology has been developed. The presented test array provides long rows and columns and allows to evaluate their parasitic effects, thereby anticipating a megapixel array to be fabricated in a subsequent development stage. Two different pixel variants have been implemented, optimized for minimum area consumption. The photosensitive thin film system consists of either a nip or a metal-ip-TCO structure, where the latter provides a better local contrast.

The dynamic range is above 60 dB and the sensitivity is 8.6 V lx^{-1} sec^{-1} for either thin film option. Pixel-to-pixel and column-to-column fixed pattern noise is largely suppressed by CDS and DDS, respectively, both performed on-chip.

HIRISE II demonstrates the benefits of TFA technology, as image sensors for digital photography have to keep pace with customer's expectations of higher resolution, fewer parasitic effects, lower power consumption and smaller price. CMOS may provide better overall performance than CCDs, considering the use of standard technology, lower supply voltages and the feasibility of on-chip image processing. However, the sensitivity loss due to the lateral integration and process downscaling are inherent drawbacks of CMOS. The 3D integration of TFA overcomes these problems, and the underlying basic circuit concepts of HIRISE II and other TFA sensors can easily be transferred to deep submicron processes. Furthermore, amorphous silicon detectors allow the recognition of three colors in one pixel. It is expected that TFA will be employed in a broad range of consumer as well as industrial and scientific applications.

References

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Fig. 13: Image taken with HIRISE II